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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/655,937	09/06/2000	Jong Sang Baek	8733.289.00	8624
30827	7590	04/06/2004	EXAMINER	
MCKENNA LONG & ALDRIDGE LLP 1900 K STREET, NW WASHINGTON, DC 20006			NELSON, ALECIA DIANE	
			ART UNIT	PAPER NUMBER
			2675	
DATE MAILED: 04/06/2004				

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/655,937	BAEK ET AL.
Examiner	Art Unit	
Alecia D. Nelson	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 21 January 2004.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-21 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351 (a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. ***Claims 1, 2, 4, 6, 8, 9, 11, 20, and 21*** are rejected under 35 U.S.C. 102(e) as being anticipated by Shin (U.S. Patent No. 6,323,836). With reference to **claims 1, 8, and 20**, Shin teaches a liquid crystal display device (100), comprising a line memory (230) for dividing a data for at least one line inputted from the exterior thereof into a plurality of groups to store the divided data therein and for outputting the data at a desired unit from each of the groups; a driving circuit (270) including n driver integrated circuits (240, 250) that are connected to the line memory (230) and the liquid crystal display panel (100) to drive the liquid crystal display panel in response to the data outputted from the line memory (230); and a timing controller (220), being connected to the line memory (230) and the driving circuit (270), for receiving a data clock inputted

from the exterior thereof to output the data from the plurality of groups of the line memory (230) to the driving circuit (270) every period of the data clock in response to a time corresponding to the number of said groups (see column 5, line 18-column 6, line 18). With further reference to claims 8 and 20, Shin teaches, with reference to the summary of the invention, generating a first data clock by frequency-dividing the data clock at a frequency-division ratio corresponding to the number of divided groups (see column 3, lines 53-62).

With reference to **claims 2 and 9**, Shin teaches, with reference to FIG. 4, a first group (A) and a second group (B), wherein the data driver ICs are divided also into the two groups (A, B) and the video data are sent to and latched at the two groups (see col. 2, lines 43-54).

With reference to **claims 4, 6, and 11**, Shin teaches, with reference to FIG 5, that the data driver ICs are divided into two groups. One group, an odd data driver IC group (32), is the driver for ICs connected with the odd numbered data lines. The other group, an even data driver IC group (33), is for the driver ICs connected to the even numbered data lines (see column 2, lines 56-64).

With reference to **claim 21**, Shin teaches that the data storage step includes sequentially receiving at least two pixel data (odd, even) to divide and store the data for one line into two groups; the frequency division ration at the data clock generating step

is two; and the two groups at the data storage step individually output the two pixel data at a desired time difference during one period of the second data clock (see column 5, line 59-column 6, line 18).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. **Claims 3, 5, 7, 10, and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin, as applied to **claim 1** above, and further in view of Nakano et al. (U.S. Patent 6,229,513).

Shin teaches all that is required as explained above with reference to **claim 1**, however fails to specifically teach that the timing controller generates an inverted data clock having a phase contrary to the input data clock and outputs a data from the first group of the line memory in response to the data clock while outputting a data from the second memory group of the line memory in response to the inverted data clock, thereby outputting the data in the first group and the data in the second group to the driving circuit at a different time during each period of the data clock.

Nakano et al. teaches that a clock signal (CK) is transmitted from the computer side and is divided by a D-type flip-flop (111) such that clock signals (D4, D5) are outputted from a non-inverting output terminal, and an inverting output terminal of the flip-flop (111), respectively. Also originally ordered display data transmitted from the computer side are inputted to a first, or second, memory (112, 113). The memory stores display data of an amount corresponding to a total number of drain signal lines connected to two drain drivers. The originally ordered display data transmitted from the computer side are first written into the first memory (112). When $2n$ display data are stored in the first memory (112), next $2n$ data transmitted are written into the second memory (113), and meanwhile the display data are read from the first memory (112) and outputted to the drain drivers (130) (see column 6, line 64-column 7, line 42).

Therefore it would have been obvious to one having ordinary skill in the art to allow the usage of circuitry included in the data control unit for outputting data from the memories according to a first and second clock signal, as taught by Nakano et al., wherein the circuitry is a part of the timing controller as taught by Shin, thereby allowing transmission of the display data from the timing controller to the drivers without increasing the bus width of the display data bus line. This reduces the amount of generated EMI thereby enhancing the resolution of the display panel.

6. **Claims 13-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al. in view of applicant's admittance of prior art.

With reference to **claims 13, 15-19**, Nakano et al. teaches a liquid crystal apparatus having a display control means for generating control signals including at least clock signals based on input display control signals inputted thereto and sending the control signals to the driving means (see abstract). The liquid crystal display apparatus comprises a first and second memory (112, 113) for receiving and storing originally ordered display data transmitted from the computer side. The data is then outputted to the drain drivers (130) through the display data bus line (134) (see column 7, lines 3-17). Drivers (130) including a group A (odd numbered) and a group B (even numbered) are connected between the liquid crystal panel (10) and the memory (112, 113) comprised in the display control unit (110) (see column 6, lines 16-37). Within the display control unit (110) a clock signal (CK) is transmitted from the computer side, and is divided by a D-type flip-flop (11) such that clock signals (D4, D5) are half the

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frequency of the original clock signal (CK). It is also taught that the generated clock signal (D4) is used for latching display data, and the second clock signal (D5) has the same frequency as and a different phase from the first clock signal (D4), which means that clock signal (D5) is an inverted version of clock signal (D4) (see column 6, lines 24-31).

Nakano et al. fails to specifically teach that the memory receives two-pixel data unit, or that the driving circuit includes n driver integrated circuits. Nakano et al. does however teach that the first and second memories (112, 113) stores display data of an amount corresponding to a total number (2n) of the drain signal lines (D) connected to two drain drivers (130). Further, with reference to a second embodiment, a liquid crystal display of higher resolution has two bus lines (134a, b) as display data bus lines, and drain drivers (130') are connected thereto (see column 7, lines 43-50).

Moreover, and with reference to **claims 14**, applicant's admittance of prior art teaches a conventional four-port data transmission method wherein n driver IC's are connected to the liquid crystal display panel are two-division driven into left and right groups (see page 4, line 18-page 5, line 5).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to combine the four-port driving method as taught by the applicant's admittance of prior art with the system as taught by Nakano et al. which suggest such driving technique in order to provide a liquid crystal display panel in which the video data of two data lines can be driven simultaneously, thereby improving the display quality of the liquid crystal display.

Response to Arguments

7. Applicant's arguments filed 1/21/04 have been fully considered but they are not persuasive. With reference to the applicant's arguments of the applied rejection to independent **claims 1, 8, and 20**, the applicant argues that the usage of the phrase "very similar" in the "Response to Arguments" of the previous response negates the anticipation of the rejection applied to the claims. However, what is included in the "Response to Arguments" is an explanation of the examiner's position and not the rejection itself. Furthermore, "similar" is defined as having characteristics in common; strictly comparable; alike in substance or essentials; or being of close resemblances. Therefore the usage of the "very similar" is just another way of stating that the invention disclosed by Shin anticipates the limitations as claimed. Further the applicant states that **claims 1 and 8** do not recite any element suggesting that data is outputted every period of a clock signal generated from an externally inputted clock signal, or any analog thereof, and reiterates **claims 1 and 8** as requiring a timing controller receiving a data clock inputted from the exterior thereof to output data to the driving circuit every period of the data clock. However, according to what is disclosed in Figure 6, data is output to the driving circuit every period of the data clocks SSC1 and SSC2, as opposed to DCK1. Furthermore, the conventional art, which is disclosed by the applicant, teaches data being output to the driving circuit every period of the data clock received externally thereof in Figures 2 and 3. Moreover, the claim recites that the timing controller receives a *data clock* inputted from the exterior thereof, and the driving circuit

outputs data every period of *the data clock*. The claim does not recite *the data clock* as *said data clock*, which would be that which is inputted from the exterior. *The data clock* is the data clock in which the driving circuit outputs data according to. Also with reference to **Claim 20**, the applicant argues that Shin is entirely silent with respect to a data clock generating step of frequency-dividing an input first data clock to generate a second data clock and a data outputting step of outputting a desired data unit from each of the groups at a different time during one period of the second data clock. However, as stated above with reference to column 3, lines 53-62, Shin teaches a driving circuit for including a clock generator for processing a first clock signal to output a second clock signal, the clock speed of the second clock signal being one Nth of that of the first clock signal. Therefore teaching that which is recited by **claim 20**. With reference to the applicant's arguments of the applied rejection to independent **claims 13 and 18**, that there is no reason to combine the teachings of the applied art to arrive at the claimed invention. However Nakano et al. teaches all that is required by the claim except, that the memory receives two-pixel data unit, or that the driving circuit includes n driver integrated circuits, but teaches with reference to a different embodiment that the first and second memories (112, 113) stores display data of an amount corresponding to a total number ($2n$) of the drain signal lines (D) connected to two drain drivers (130). Therefore there is a suggestion that it is possible for the memory to receive two pixel data units from the exterior thereof and dividing the data for at least one line into a plurality of groups to store the divided data therein and for outputting the two pixel data unit from each of the groups, since it is possible for the memories to store display data

of an amount corresponding to the total number of the drain signal lines, in order to increase the resolution of the driven display, which is also the reason as given by the applicant's teaching of related prior art. Further, applicant briefly states that the teachings of the related prior art did not cure the deficiencies of Nakano et al., but fail to go into detail as to why. Therefore the rejection as applied to the claims will be maintained.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703) 305-0143. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras can be reached on (703) 305-9720. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

adn/ADN
April 5, 2004



4-5-2004